

## TRANSMITTAL LETTER TO THE UNITED STATES

0522-1752

DESIGNATED/ELECTED OFFICE (DO/EO/US)

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR 1.5)

CONCERNING A FILING UNDER 35 U.S.C. 371

09/890376

INTERNATIONAL APPLICATION NO.

INTERNATIONAL FILING DATE

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PCT/EP00/00586

January 26, 2000

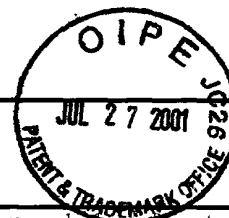
January 27, 1999

TITLE OF INVENTION

METHOD FOR FABRICATING THIN FILM SEMICONDUCTOR DEVICES

APPLICANT(S) FOR DO/EO/US

Jorg Horzel and Eva Yazsonyi



Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
  - a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
  - b. ☒ has been transmitted by the International Bureau
  - c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ A copy of the International Search Report (PCT/ISA/210)
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
  - a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau)
  - b. ☐ have been transmitted by the International Bureau
  - c. ☐ have not been made, however, the time limit for making such amendments has NOT expired
  - d. ☒ have not been made and will not be made
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4))
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

## Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment
17. ☐ A substitute specification
18. ☐ A change of power of attorney and/or address letter.
19. ☐ Certificate of Mailing by Express Mail
20. ☐ Other items or information

U.S. APPLICATION NO. (UNKNOWN - SEE 37 CFR 1.5) <div style="font-size: 2em; font-weight: bold; margin-top: 5px;">097/890376</div>	INTERNATIONAL APPLICATION NO <div style="font-weight: bold; margin-top: 5px;">PCT/EP00/00586</div>	ATTORNEY'S DOCKET NUMBER <div style="font-weight: bold; margin-top: 5px;">0522-1752</div>
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21. The following fees are submitted <b>BASIC NATIONAL FEE ( 37 CFR 1.492 (a) (1) - (5)) :</b>				CALCULATIONS    PTO USE ONLY	
<input type="checkbox"/> Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO . . . . .				\$1,000.00	
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO . . . . .				\$860.00	
<input type="checkbox"/> International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO . . . . .				\$710.00	
<input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) . . . . .				\$690.00	
<input type="checkbox"/> International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) . . . . .				\$100.00	
<b>ENTER APPROPRIATE BASIC FEE AMOUNT =</b>				\$860.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (e))				\$0.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	17 - 20 =	0	x \$18 00	\$0.00	
Independent claims	2 - 3 =	0	x \$80 00	\$0.00	
Multiple Dependent Claims (check if applicable). <input type="checkbox"/>				\$0.00	
<b>TOTAL OF ABOVE CALCULATIONS =</b>				\$860.00	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) (check if applicable). <input type="checkbox"/>				\$0.00	
<b>SUBTOTAL =</b>				\$860.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492 (f))				\$0.00	
<b>TOTAL NATIONAL FEE =</b>				\$860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) (check if applicable). <input type="checkbox"/>				\$0.00	
<b>TOTAL FEES ENCLOSED =</b>				\$860.00	
				Amount to be: refunded	\$
				charged	\$

☒ A check in the amount of **\$860.00** to cover the above fees is enclosed

☐ Please charge my Deposit Account No. \_\_\_\_\_ in the amount of \_\_\_\_\_ to cover the above fees.  
 A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No **12-0913** A duplicate copy of this sheet is enclosed.

**NOTE:** Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO  William M. Lee, Jr. Lee, Mann, Smith, McWilliams, Sweeney & Ohlson Post Office Box 2786 Chicago, Illinois 60690-2786	<div style="text-align: center;">                       SIGNATURE                 </div> <div style="text-align: center;">                     William M. Lee, Jr.                      NAME                 </div> <div style="text-align: center;">                     26,935                      REGISTRATION NUMBER                 </div> <div style="text-align: center;">                     July 27, 2001                      DATE                 </div>
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IN THE UNITED STATES PATENT AND  
TRADEMARK OFFICE

In the application of:

Jorg Horzel & Eva Yazsonyi

Serial No.: Unassigned

Filed: Unassigned

Examiner:

Art Unit:

Docket No. 0522-1001

For: METHOD FOR FABRICATING THIN  
FILM SEMICONDUCTOR DEVICES

AMENDMENT ACCOMPANYING APPLICATION

Honorable Director of  
Patents and Trademarks  
Washington, D.C. 20231

Dear Sir,

The present application is the National Filing of International Application No. PCT/EP00/00586. Before calculation of the National Filing fee for the United States, it is requested that the application be amended as follows:

In the Claims

Cancel claims 1-18 of the International Application, and substitute new claims 19-35 as follows:

19. A method for fabricating a solar cell on a reusable substrate of a semiconductor material comprising the steps of:

- providing a substrate of a semiconductor material having at least one surface;
- forming at least one porous layer on said surface of said substrate;
- depositing at least one semiconductor layer on said porous layer;
- forming active devices in said semiconductor layer including forming at least one n-type doped region and at least one p-type doped region in said semiconductor layer of each active device, said n-type and p-type regions having an exposed surface;

forming electrical contacts to said active devices including forming metal contacts to the exposed surfaces of said n-type region and said p-type region of said active devices;

attaching a support to the surface overlying said metal connections; and

non-mechanically detaching said substrate from said semiconductor layer by removing said porous layer with a wet chemical etch using said support as an etch mask.

20. A method as recited in claim 19, wherein said porous layer on said surface of said substrate is formed by an electroless etching technique in an aqueous chemical solution.

21. A method as recited in claim 19, wherein said surface of said substrate is textured or structured prior to forming said porous semiconductor layer.

22. A method as recited in claim 19, wherein said support is a flexible sheet material.

23. A method according to claim 19, wherein said support is composed of a plastic or a polymer.

24. A method according to claim 19, wherein said porous layer is a single porous semiconductor layer.

25. A method as recited in claim 24, wherein said single porous semiconductor layer is formed such that there is a gradient in porosity.

26. A method as recited in claim 24, wherein said porous semiconductor layer is a porous silicon layer, said method further comprising the step of thermally oxidizing said porous silicon layer to thereby convert said porous silicon layer to a porous silicon oxide layer.

27. A method as recited in claim 26, wherein said substrate is detached from said semiconductor layer by removing said porous silicon oxide layer using a wet chemical etch, said wet chemical etch being selective to said substrate and said semiconductor layer.

28. A method as recited in claim 19, wherein said metal contacts are formed by screen printing a first metal paste to contact said p-type doped regions and a second metal paste to contact said n-type doped regions.

29. A method according to claim 19, wherein said semiconductor material of said substrate is selected from the group consisting of Si, SiGe, Ge, GaAs.

30. A method as recited in claim 29, wherein said substrate is doped with either an n-type impurity or a p-type impurity, said substrate having a highly doped surface region whereon said porous layer will be formed.

31. A method according to claim 19, wherein each of said semiconductor layers is either an n-type or a p-type doped layer being composed of a semiconductor material selected from the group consisting of Si, Ge, SiGe, GaAs.

32. A method as recited in claim 31, wherein said thin film semiconductor devices are thin film solar cells having a plurality of actively collecting semiconductor layers of different doping types.

33. A method according to claim 19, wherein after detaching said substrate an additional layer is formed on exposed parts of said semiconductor layer, said additional layer being used at least as a passivation layer or an anti-reflective coating layer or a back surface reflector layer.

34. A method for fabricating a solar cell device on a reusable substrate of a semiconductor material comprising the steps of

providing a substrate of a semiconductor material having a first major surface, a second major surface, opposite to said first major surface, and edge surfaces;

forming at least one porous semiconductor layer on each of said major surfaces and said edge surfaces of said substrate by an electroless etching technique in an aqueous chemical solution;

depositing at least one semiconductor layer on said porous semiconductor layer;

forming active devices at least in the semiconductor layers formed on said first major surface of the substrate including forming at least one n-type doped region and at

least one p-type doped region in said semiconductor layer formed on said first major surface of each active device, said n-type and p-type regions having an exposed surface;

forming metal contacts at said first surface of said substrate contacting said active devices including forming metal contacts to the exposed surfaces of said n-type region and said p-type region of said active devices;

attaching a support to the surface overlying said metal connections;

removing at least the semiconductor layers formed at the edge surfaces of the substrate to thereby expose the edges of the porous semiconductor layers; and

non-mechanically detaching said substrate from said semiconductor layer by removing said porous layer with a wet chemical etch using said support as an etch mask.

35. A method as recited in claim 34, wherein thin film semiconductor devices are fabricated both in the semiconductor layers formed on said first major surface of the substrate and on said second major surface of the substrate.

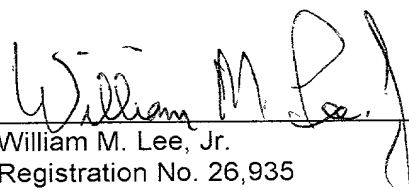
#### REMARKS

The above amendments have been made in order to eliminate multiple dependency from the application before calculation of the application filing fee. The claims correspond to the claims original in the International Application, except that correction.

Examination of the application on its merits is awaited.

Respectfully submitted,

Date: July 23, 2001

  
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William M. Lee, Jr.  
Registration No. 26,935  
Lee, Mann, Smith, McWilliams, Sweeney  
& Ohlson  
P.O. Box 2786  
Chicago, Illinois 60690-2786  
(312) 368-1300 Telephone  
(312) 368-0034 Facsimile

## METHOD FOR FABRICATING THIN FILM SEMICONDUCTOR DEVICES.

## FIELD OF THE INVENTION

- 5 The present invention is related to semiconductor processing techniques for fabricating thin film semiconductor devices. Examples of such thin film semiconductor devices are for instance power devices and opto-electronic devices like e.g. solar cells.

## BACKGROUND OF THE INVENTION

- 10 Today's solar cell production is dominated by silicon based solar cells. So far, most of the produced solar cells use relatively thick crystalline Si substrates of typically 200  $\mu\text{m}$  thickness or more. On the other hand, amorphous Si solar cells suffer from modest conversion efficiencies and unavoidable degradation effects. Irrespective of the solar cell concept used, nowadays the cost of the produced solar energy is for all
- 15 state-of-the-art devices too high to compete with conventional energy sources. Particularly, for solar cells using thick crystalline Si substrates, having clearly the largest market share, the cost per Watt of produced energy is mainly dominated by the high substrate cost for mono- or multi-crystalline substrates. This substrate price cannot be influenced too much since good quality Si material is required to obtain
- 20 desirable solar cell conversion efficiencies. Additionally this substrate price depends on developments in the micro-electronics industry since waste material from this industry is used to produce substrates for solar cells. By using adequate deposition techniques, like for instance a chemical or physical vapor deposition technique, very thin solar cells can be formed. The ability to make high-quality thin solar cells can lead
- 25 to in a clear cost reduction and make prices and availability of substrates more independent from other industries.

- Provided that one succeeds to diminish the substrate cost substantially and that the processing costs can further be limited by introducing as much as possible simple and cheap processing techniques, cost projections assuming a reasonable solar cell
- 30 conversion efficiency of better than 10 % show that solar energy would become competitive with conventional energy sources which could lead to a break-through for this environmentally benign energy source. Furthermore, the use of thin film solar cells of a few  $\mu\text{m}$  thickness in conjunction with a plastic or polymeric support film, makes

these cells very flexible and offers therefore a wider range of applications than thick crystalline Si substrates.

EP 0797258 is related to a method of making a thin film solar cell. The thin film is formed on a multi-layer porous structure having at least two layers of different porosity. This porous structure is formed on a semiconductor substrate by anodization. However anodization is known as an effective but complex technique which amongst others has a negative impact on the overall throughput of the fabrication process. As a consequence, such a technique is less suited for mass production. According to EP 0797258, the thin film can be mechanically separated from the substrate along a line of weakness defined in the porous structure. A drawback of this separation technique is that it is not suited for mass production, particularly when using techniques such as screen printing on the surface, because this inherent built-in mechanical instability will lead to yield problems. Due to this mechanical instability the thin film can be unintentionally detached from the substrate prior to the intended separation. On the other hand, if the mechanical force, required to separate the thin film from the substrate is high, i.e. the attachment is mechanically more stable, then this might cause stress and damage in the thin film layer during the separation process which leads to a deterioration of the device performance.

US 5,856,229 describes a process for producing a semiconductor substrate (rather than a completed device) which comprises steps of forming a porous layer on a first substrate, forming non-porous monocrystalline semiconductor layer on the porous layer, bonding the non-porous monocrystalline layer onto a second substrate, separating the bonded substrates at the porous layer, removing the porous layer on the second substrate, and removing the porous layer constituting the first substrate. This known technique is limited to the separation of a monocrystalline layer with active devices from the first substrate. There is no indication that the method of etching a porous layer might find advantageous use after active devices have been formed in the monocrystalline layer, in fact the whole purpose of this known method is to provide a substrate which can subsequently be used to form a device.

WO 99/01893 describes a method of producing layered structures on a substrate having a porous layer and one or more non-porous layers. The non-porous layers are separated from the substrate by mechanically breaking the porous layer. There is no indication that a chemical etching technique could replace the mechanical



separation method, nor is there any hint that such an etching technique would have any expectation of success. Generally, protracted etching steps are not preferred.

## OBJECTS OF THE INVENTION

5 It is an object of the invention to fabricate thin film semiconductor devices on a substrate which can be recycled after detaching it from the thin film semiconductor device in order to diminish the substrate cost substantially.

Another object of the invention is to introduce as much as possible simple, cheap and particularly highly reliable processing techniques during the fabrication of these thin film semiconductor device. Furthermore, the use of thin film solar cells of a few  $\mu\text{m}$  thickness in conjunction with a plastic or polymeric support film, makes these cells very flexible and offers therefore a wider range of applications than thick crystalline Si substrates.

10 It is a further object of the invention to introduce a highly reliable method to separate the thin film semiconductor devices from the reusable substrate. Preferably these thin film semiconductor devices are already fully processed, i.e. fully contacted and attached to a support, before detachment from the substrate.

## SUMMARY OF THE INVENTION

20 The invention relates to a method for the fabrication of thin film semiconductor devices at low cost. Examples of such devices are for instance solar cells, light emitting diodes and power devices. Also the use of semitransparent thin film solar cells for shading purposes seems to be feasible with the invented technique. Particularly, a method is disclosed for fabricating thin film semiconductor devices on a

25 reusable substrate of a semiconductor material comprising the steps of:

providing a substrate of a semiconductor material having at least one surface;

forming at least one porous layer on said surface of said substrate;

depositing at least one semiconductor layer on said porous layer;

forming active devices in said semiconductor layer;

30 forming electrical contacts to said active devices;

attaching a support to the surface overlying said metal connections; and

non-mechanically detaching said substrate from said semiconductor layer by removing said porous layer with a wet chemical etch using said support as an

etch mask.

The invented method allows for simple and cheap processing techniques as screen printing to be successfully applied in combination with thin solar cells of only a few  $\mu\text{m}$  thickness using very cheap supports such as plastic films. The whole process is executed on a high quality substrate that is well compatible with all high temperature treatments as diffusion and thermal oxidation. The thin film semiconductor devices are lifted off from this comparably expensive substrate at the end of the process after being attached to a cheap second substrate, i.e. the support. The expensive high quality substrate is recycled and can be used for many processing cycles. Therefore the substrate is not contributing very much to the general processing cost. For simplicity and clarity, in the following description and examples the thin film semiconductor devices will be limited mainly to Si solar cells, but the invention is in no way limited to thin film solar cells.

According to the method of the present invention, optionally first a structuring or texturing of the substrate can be performed. This texturing might be kept for several processing cycles and will be found back as negative profile on the thin film solar cell. After cleaning the substrate, at least one porous semiconductor layer can be formed on a surface of the substrate. Particularly, a single porous semiconductor layer can be formed having a uniform porosity or a gradient in porosity. Preferably this porous semiconductor layer is formed in one processing step by an electroless etching technique in an aqueous chemical solution. For instance a solution of  $\text{H}_2\text{O}$ ,  $\text{HF}$  and  $\text{HNO}_3$  can be used. Also other solutions known in the art can be used. Optionally this porous layer can be oxidized to form a kind of amorphous or porous  $\text{SiO}_2$  layer. The intention is to remove these porous Si or  $\text{SiO}_2$  layers at the end of the process in order to detach the thin film Si solar cells from the substrate. This can for instance be achieved by under-etching the thin films by solutions that etch the porous film at rather high etch rates selectively away. The detachment is however only executed at the end of the processing sequence to benefit from firm attachment to the substrate during processing. As a consequence, the thin film contains a plurality of semiconductor devices which are basically completed, fully contacted and attached to a support. Afterwards, primarily only a separation step in order to detach the thin film from the substrate and a dicing step to separate the thin film devices one from another is required. This separation step is quite a challenge because dependent on the size of the

substrate, e.g. a 150 mm diameter silicon wafer, one requires a process which allows to perform a lateral etch over several centimeters to remove the comparably thin porous layer, i.e. typically between 0.5 and 5  $\mu\text{m}$ , in order to separate the thin film from the substrate. Moreover this etch process has to remove this porous layer in a selective way especially with respect to the thin film and the semiconductor devices therein but preferably also with respect to the substrate. The method of the present invention surprisingly succeeds to meet all the aforementioned requirements amongst others because the support is used as an etch mask to protect the semiconductor devices during the non-mechanical removal step.

By using a high quality Si-containing substrate high temperature processing steps such as the chemical vapor deposition of Si, the diffusion and thermal oxidation of the thin film surface can be performed as for usual processing on thick crystalline Si substrates without fearing degradation in the minority carrier life time or contamination caused by the substrate. Also other high quality semiconductor substrates such as Ge or GaAs substrates can be used.

At least one semiconductor layer, defining a thin film, is deposited onto the porous surface layers by adequate deposition techniques. Particularly, crystalline Si layers of acceptable quality can be formed using a chemical vapor deposition technique. During deposition these layers can already be doped in order to create one or more p-n junctions in the thin film by switching between different gas atmospheres using different doping gasses. Additionally impurities can be diffused at the exposed thin film surface to form further junctions or highly doped contact regions. This can be done in a selective way as described in applicant's PCT patent application WO 98/28798 which is hereby incorporated by reference.

Solar cells can be formed in the thin film semiconductor layers comprising at least one n-type doped region and at least one p-type doped region in these semiconductor layers. Particularly both n-type and p-type doped regions can be contacted at the same surface. The exposed surface will be passivated typically by using thermal oxidation and/or  $\text{SiN}_x\text{H}_y$  deposition steps. The  $\text{SiN}_x\text{H}_y$  deposition can at the same time lead to a bulk passivation in the thin film if it is followed subsequently by a high temperature step. As for example, the short high temperature firing step for forming printed metal connections contacting the n-type and p-type regions. The metallisation is preferably performed by simple industrially applicable techniques such

as screen printing of metal pastes. Contact to the n-type doped region is typically made by printing a pattern of Ag paste. Contact to p-type doped regions is typically made by printing a pattern of an Al, an Ag or an AgAl paste. The pastes are dried after printing and subsequently co-fired at elevated firing temperatures. During this short firing step not only good electrical contacts are formed to the differently doped regions, but also hydrogen will effuse from the  $\text{SiN}_x\text{H}_y$  layer into the thin film bulk region to passivate possible defects (as for instance at grain boundaries when poly-crystalline Si was deposited). After metallisation, the solar cell is functionally completed.

In case the final solar cell device will be used as back contact solar cell and therefore only the non-metallised surface will be illuminated as front surface of the device, a back surface reflector (BSR) might result in better light trapping properties and therefore better solar cell conversion efficiencies. This BSR might be applied optionally by first printing an electrically isolating paste (polymeric paste for instance) over one of the electrode metallisation patterns to thereby short circuiting the device when a metal is applied as BSR. Particularly, a highly reflective metal film can be applied over the whole back surface using techniques like evaporation or electroless plating. In case a non-conductive material of good reflectivity is used as BSR, this electrically isolating paste can be omitted. A BSR has however not necessarily to be formed directly in contact with the thin film solar cell. The use of a reflective layer as back sheet of a finished solar cell module might result in similar or better light trapping properties (depending on the used passivation layers on the rear surface) without asking for additional processing steps or cost.

At this stage of the process the substrate fulfills all tasks to have a simple and reliable processing sequence. Before lifting off the thin film however another substrate has to be attached to it as a support. This is preferably a cheap and flexible plastic or polymeric film, that can be applied by screen printing technology as well. A polymeric paste can be printed and subsequently dried at temperatures around 200 degrees C. Optionally this plastic film can be transparent. The support can be also attached by using an adhesive film in between the support and the thin film.

Finally the thin film solar cell with the support attached to it is detached from the substrate. The detached substrate is then subjected to a recycling step and is used for many further processing cycles. The detachment can be realized by under-etching the thin film solar cell with chemical etching solutions that remove selectively the

porous semiconductor or oxidized porous semiconductor layers and using the support as an etch mask. The support may be a flexible sheet material such as a plastic or a polymer.

After detaching the thin film solar cell from the substrate the exposed surface of the thin film can be processed additionally. This might be for instance a  $\text{SiN}_x$  deposition at moderate temperatures, i.e. compatible with the support e.g. 200 degree C for a plastic or polymeric support. The  $\text{SiN}_x$  layer might serve as a passivation layer for this surface but also at the same time as an anti-reflective coating layer when the solar cell is used as a back contact solar cell. If the non-metallised surface however is used as back surface, an additional BSR layer might be applied optionally on this surface to achieve better light trapping.

Module interconnection of thin film semiconductor devices that are produced in the described way is simpler than for conventional thick Si substrates since both terminals are located on the same substrate surface and no connections have to be formed from front to rear surfaces. The interconnection can be done as for usual solar cell modules by using solder coated Cu strips that might be soldered to the busbars of n-type and p-type electrodes. This can be done already prior to the attachment of the plastic or polymeric support and the subsequent detachment of the thin film solar cells. It is however also possible to form openings at terminals in the support after finishing the process completely. Also monolithic module interconnection seems feasible.

All processing steps that have to be applied in this thin film solar cell process are simple and at low processing cost and can lead to high throughput. The final cost for the solar cell will mainly depend on the thin film deposition technique that is used. Calculations show that the cost per Watt of solar energy can be drastically reduced by applying such a process to less than 30% of the cost of today's industrially produced solar cells. This will mean a major break through of solar cell technology.

#### BRIEF DESCRIPTION OF THE DRAWINGS

All drawings are primarily for better illustration of the main features and are not to scale. The devices and fabrication steps are depicted in a simplified way for the sake of better visibility. Not all alternatives and options are depicted in the figures and therefore the invention is in no way limited to the fabrication steps or device structures presented in those figures. For simplicity the figures are also limited to only half of the

substrate. The method of the present invention is suited to form symmetrically on both major surfaces of the substrate exactly the same structures.

Figure 1 depicts, according to an embodiment of the invention, a schematic process flow for fabricating a simple thin film Si solar. A set of processing steps is depicted in figure 1 a) to figure 1 o).

Figure 2 depicts, according to the second embodiment of the invention, a schematic representation of a thin film Si solar cell with a grown floating layer (21) on the substrate before detachment from the substrate.

Figure 3 depicts, according to the third embodiment of the invention, a schematic representation of a thin film Si multi-layer solar cell with two layers of opposite doping type. Both demonstrated devices are still attached to the substrate prior to the detachment step.

Figure 3 a) depicts, according to this third embodiment of the invention, a thin film Si multi-layer solar cell with a n-type layer (31) and a p-type layer thereon(32). This n-type layer (31) is selectively connected by means of a highly doped n-type region (33).

Figure 3 b) depicts, according to this third embodiment of the invention, a thin film Si multi-layer solar cell with a p-type layer (36), a n-type layer (37) and again a p-type layer (38) thereon. This n-type layer (37) is selectively connected by means of a highly doped n-type region (33) and the p-type layer (36) is selectively connected by means of a highly doped p-type region (39).

Figure 4 depicts, according to the fourth embodiment of the invention, a schematic representation of a thin film Si multi-layer solar cell with a plurality of layers of alternating and opposite doping type. All p-type layers (42) are connected by means of a highly doped p-type connection region (44), all n-type layers (41) are connected by means of a highly doped n-type connection region (43). The depicted structure is detached from the substrate.

#### DETAILED DESCRIPTION OF THE INVENTION

In relation to the appended drawings the present invention is described in detail in the sequel. It is apparent however that a person skilled in the art can imagine several other equivalent embodiments or other ways of executing the present invention, the spirit and scope of the present invention being limited only by the terms of the

appended claims. Therefore, although the method of the present invention to form thin film semiconductor devices with a simple and cheap process is not limited to Si solar cells the following description of some embodiments will be limited for simplicity and clarity to Si solar cells.

5 It should be noted that high temperature steps can enhance the quality of Si thin film, provided that defects in the thin film diffuse at considerably high rates during such high temperature treatments. In that case the defects can diffuse to the porous Si layer or to the high quality low defect density Si substrate having and get trapped.

10 In a preferred embodiment of the invention, as in figure 1, a method is disclosed for fabricating thin film solar cells on a reusable Si substrate. Preferably a mono-crystalline Si substrate (1) (Fig. 1 a)) of good quality with respect to the purity of the Si (high minority carrier life time) is chosen to serve as a substrate during thin film deposition and subsequent processing before the finished solar cells are detached from this substrate and the substrate is prepared in a recycling cycle to serve for many  
15 other thin film production cycles. Alternatively, also multi-crystalline Si substrates or other crystalline Si substrates of reasonably good Si quality can be used. The thick, typically 300  $\mu\text{m}$  or more, substrate has to be cleaned at the start of the process from surface contamination by means that are well known to persons skilled in the art of solar cell processing.

20 Subsequently (Fig. 1b)) the substrate surfaces can undergo an optional texturing or structuring step, creating a macroscopic structure (2) that will be found back as a negative structure on the deposited thin film after detaching the thin film solar cell at the end of the processing sequence. Even though this texturing or structuring of the surface is not required for the device formation, it will serve in the  
25 finished solar cell device as light trapping scheme, clearly improving the final solar cell conversion efficiency. The texturing or structuring of the device can be performed by methods well known in solar cell processing as random alkaline texturing, mechanical structuring or even more elaborated light trapping schemes as described in the literature. Since the mentioned macroscopic structure will be substantially the same  
30 after recycling the substrate at the end of the processing it can be used over several thin film solar cell manufacturing cycles and has not to be renewed after each process cycle.

In a next step, fig. 1c), a thin porous Si layer (3) is formed by an electroless

etching technique in an aqueous chemical solution. This chemical solution typically comprises water ( $H_2O$ ), hydrofluoric acid (HF), and nitric acid ( $HNO_3$ ). Additives, such as PVA (polyvinyl alcohol) or PVP (polyvinyl pyridine) or other additives known to persons skilled in the art, that might improve the homogeneity of the porous Si film.

5 An electroless etching step for porous silicon formation can be performed on many substrates simultaneously. For instance, a plurality of substrates can be immersed in a tank with the aqueous chemical solution. This yields a high throughput, good controllability and homogeneity. On the other hand, a galvanic porous silicon formation technique requires to contact the substrates to an electrode which  
10 incompatible with the requirement for a high throughput and therefore makes this technique less suitable for industrial application. The porous Si layer is used as a sacrificial layer and will be removed at the end of the process. During processing it might serve for gettering impurities and defects from the deposited thin film. These impurities and defects might diffuse into the much larger bulk Si substrate having a  
15 very low concentration of impurities and defects or they might be trapped on the huge surface area of the porous layer. The latter holds especially if the porous Si layer and/or the underlying substrate are highly doped by phosphorous which is well known by persons skilled in the art of solar cell processing to trap impurities and defects during gettering.

20 The surface concentration of either n-type impurities or p-type impurities in the porous Si film might optionally be intentionally increased. This step can be executed after or prior to the porous Si formation. The first option has the advantage that extremely high doping impurity concentrations can be achieved by the huge surface area that interacts with the diffusion source. The latter option has the advantage that  
25 the surface layer of the substrate has a different doping than the bulk of this substrate. This allows during porous Si formation for structures of completely different porosity in the diffused top region and the bulk region just below. Such a double structure in the porous film might facilitate the detachment of the thin film Si solar cell at the end of the process.

30 The porous Si formation step can be optionally followed by a thermal oxidation step or an oxide deposition step. During thermal oxidation the porous Si layer is transformed in an  $SiO_2$  film that might be still porous or amorphous in its structure. Such a film can be under-etched selectively at the end of the process using a wet



chemical etch based on e.g. concentrated HF solutions. Growing a Si thin film on a SiO<sub>2</sub> layer will however result in a poly-crystalline structure of this film, while the growth on porous Si directly allows to reproduce the mono-crystallinity of the substrate.

5 An embodiment of a method in accordance with the present invention of forming a porous Si layer in a surface region of the substrate with a electroless porous Si formation solution will now be described. A batch of Si host substrates are immersed in a solution comprising hydrofluoric acid HF (50 %) and nitric acid HNO<sub>3</sub> (70%). Concentrations of 100 – 5000 parts of HF to 1 part HNO<sub>3</sub> are preferred for the  
10 formation process. Additives known to persons skilled in the art such as PVP or PVA that help the wettability of the substrate surface may be added in small amounts to the mentioned solution. Typical etching times for porous Si formation are in the range of 1-5 minutes. The mentioned solution can be easily replenished by compensating for the HNO<sub>3</sub> that is consumed during the chemical reaction. In this way the solution can be  
15 utilized for a large number of substrates and does not contribute considerably to the processing cost. The amount of consumed HNO<sub>3</sub> can be easily determined by weighing the substrates prior to and after the porous Si formation. The mass difference corresponds to the amount of etched Si. From this amount of consumed Si the reaction equation can be easily solved to determine the amount of HNO<sub>3</sub> that was taking part in  
20 the reaction. After formation of a porous Si layer on the surface of the host substrate, the porous layer may be oxidized. This oxidation of the porous layer is typically executed by a heat treatment in an oxygen containing gas atmosphere. This thermal oxidation of porous Si starts already at comparably moderate temperatures of 500 – 600 ° C, but preferably the thermal oxidation is performed at temperatures higher than  
25 700 ° C. During this treatment the porous Si layer is converted or partially converted at the surface region into a porous silicon oxide structure.

The electroless formation of a porous Si layer in a Si substrate results typically in a gradient of the porosity from the surface (very high porosity) to the interface with Si. This is not advantageous for the subsequent epitaxial growth of a monocrystalline  
30 Si thin film during CVD deposition and an underetching step after processing a thin film solar cell. Therefore, the surface region of the moderately doped substrate (typically p-type Si with a homogeneous boron concentration of around 10<sup>15</sup> atoms/cm<sup>3</sup>) is preferably doped (by a conventional thermal diffusion process for

instance or by ion implantation and activation) to a relatively high p+ doping level of typically  $10^{18}$  atoms/cm<sup>3</sup> in accordance with a further embodiment of the present invention. In this way it is possible to achieve a relatively moderate porosity in the surface region of the substrate and a much higher porosity underneath at the moderately doped bulk Si close to the surface. The chemical solutions that can be applied for forming the porous Si formation are the same as described above.

The formation of a porous surface layer for later lift-off purposes is followed by a thin film formation step, fig 1d). A Si layer (4) ranging from about one to several micrometer thickness is grown by an adequate deposition technique as for instance CVD growth of Si from gaseous sources. Temperatures for this technique are typically above 700 degrees C. The deposition technique and thickness of the final thin film can be chosen according to the final thin film structure. The light trapping properties as well as the achievable effective minority carrier life time at the end of the process determine the ideal thickness of the deposited layer. In case there is opted for oxidizing the porous silicon layer, then a thermal oxidation step can be executed during the temperature ramp-up in the Si growth system by using a oxygen containing gas atmosphere. The use of oxygen or inert gases as N<sub>2</sub> that always contain traces of oxygen being sufficient to oxidize a surface at elevated temperatures, will result in a poly-crystalline Si thin film after Si deposition. This gives however the advantage of saving processing cost because for the growth of mono-crystalline thin Si films a reducing gas atmosphere of highly pure H<sub>2</sub> is required during the temperature ramp up. Therefore the omission of highly pure H<sub>2</sub> will clearly reduce the cost of processing gasses.

Furthermore, during the thin film growth doping gasses can be controllably introduced and varied to thereby result in grown doping profiles or in junctions when different doping impurities of opposite type are introduced. To achieve steep transitions from one doping type to the other and to avoid cross doping as much as possible, the growth of Si of different types might be executed as well in locally separated processing environments (in a basically continuous deposition system with several deposition areas). Using these possibilities, junctions can virtually be located at any desirable plane in the bulk of the thin film device, that is parallel to the surface plane. This gives a lot of freedom in the choice of the final device structure of which a few are described here as exemplary embodiments. These embodiments are only

examples of advantageous use of the invention. The invention is however not limited to these exemplary embodiments, but might be used in many other variations and modifications that are obvious to persons skilled in the art.

Further, according to this first embodiment, as a first example, a p-type Si layer preferably with a high resistivity is formed using for instance boron, gallium or aluminum as doping impurity. No junction will be formed during the growth of the Si layer. Optionally a gradient or profile might be applied to have the doping concentration varying with depth in the layer. After the thin film formation on all surfaces of the substrate, a masking paste (5), preferably a dielectric paste or a paste with the same type of doping impurities as the thin film layer is printed (fig. 1e)) to those areas of the surfaces that require a metal connection to contact the p-type regions to thereby form p-type electrodes. This masking pattern might be slightly wider than the final metallisation pattern to avoid possible shunt paths between the two types of electrodes to be formed. The masking paste is dried and avoids any n-type in-diffusion at those areas. An n-type doped diffusion paste (6) is printed and subsequently dried (fig 1f)) in a manner to obtain an inter-digitated electrode structure. This pattern is similar to the final metal pattern defining the n-type electrode and is typically also chosen to be slightly wider (margin for alignment) than the final n-type electrode. During the diffusion at elevated temperatures the regions at which the diffusion paste was printed will become heavily n-type doped by diffusing for instance P from the source material into the underlying semiconductor layer thereby forming a highly doped n-type region (8). At the same time, however, P diffuses indirectly via the gas phase from the source material into those areas that are not covered by diffusion or masking pastes thereby forming a weakly doped n-type region (7) at all these areas. Alternatively, a p-type dope paste instead of a dielectric paste can be used as a masking. This can be for instance a boron paste, an Al paste or Ga paste. These pastes are able to form during diffusion p, p<sup>+</sup> or p<sup>++</sup> regions and might be additionally covered by a slightly wider pattern of masking paste, as for instance a SiO<sub>2</sub> paste, to avoid cross diffusion effects and/or low lateral shunt resistance values between p- and n-type regions.

After removing the remaining traces of paste materials the substrate surface can be passivated by a passivation step or sequence. This might include the growth of a thermal oxide layer that can passivate the surface effectively. Preferably a SiN<sub>x</sub>H<sub>y</sub>

layer (9) is deposited (fig. 1h) by techniques like plasma enhanced chemical vapor deposition (PECVD). This layer serves when used together with a short high temperature annealing step as a passivation layer for surface and bulk of the thin Si film. An example of such a temperature annealing step is e.g. the metallisation firing of screen printed contacts which is applied later in the processing. The passivation arises from atomic hydrogen being released from this  $\text{SiN}_x\text{H}_y$  layer during the temperature annealing step and effusing from this  $\text{SiN}_x\text{H}_y$  layer into the underlying semiconductor layer. The  $\text{SiN}_x\text{H}_y$  layer can be optionally deposited in addition to a thermal oxide or as the only passivation layer. Additionally it can serve as anti-reflective coating layer if this surface of the thin film device is later used as front surface of the solar cell. The passivation of the surface regions is an important requirement for the thin film devices since the relative importance of the surface region increases with decreasing device thickness. Other passivation layers well known to persons skilled in the art can also be applied alternatively or additionally to the mentioned ones.

After surface passivation both electrodes of the device have to be metallised to end up with a operational thin film solar cell. This is preferably done by using a 'firing through technique' that allows to make contact through the passivation or anti-reflective coating layers using screen printing of advanced metallisation pastes at optimized firing conditions (fig.1 i)). Typically a Ag paste is printed in alignment with the highly doped n-type regions (11) and an Ag, AgAl or Al paste (10) in alignment with the p-type regions. The pastes are individually dried and then preferably co-fired at the same time. During the firing step low resistive electrical contacts (12) and (13) are formed to the respective solar cell electrode regions as can be seen from figure 1 j) without causing shunt resistance by metal particles that might penetrate through the junction of the n-type contact region if no care is taken or when the junction depth of this n-type contact region is too shallow. Typically inter-digitating patterns of elongated contacts are used for both metallisation patterns leading to a terminal busbar region on opposite sides of the solar cell. These terminal busbars facilitate the interconnection of the thin film solar cells in modules. The thin film Si solar cell is at this stage principally finished and operational. However the quite expensive substrate is still firmly attached to it and should be used again for many subsequent processing cycles in order to reduce the processing cost considerably.

Therefore a support is applied on the metallised surface of the thin film solar

cell (see also fig. 1k). This support (14) should serve after lift-off of the thin film structure from the substrate (1) as new substrate or superstrate. The support (14) can serve at the same time as back surface reflector (BSR) if this side of the thin film solar cell is going to be used as rear surface and therefore will not be illuminated. Preferably the support should be easy to apply, cheap, flexible and it has to withstand the subsequent lift-off procedure or other subsequent processing steps. Particularly the support has to act as an etch mask or etch barrier during the non-mechanical detachment step. In other words the etch mask is a layer which at least avoids that a surface which is covered by this layer is exposed to the etch solution to thereby avoid damaging this surface during the etch process. Preferably also the etch mask itself is not or only limited affected by the etch solution. Ideally the support is a plastic or polymeric film that can be easily applied by screen printing a polymeric paste onto the surface and drying it. Also other cheap methods to attach such a support, or supports composed of a different material can be used. If the metallised surface is going to be used as front surface of the final thin film solar cell, then the support has to be a transparent superstrate film in order to allow light to enter the solar cell device.

The thin film solar cell is lifted off (fig.1 m)) from the substrate by selectively removing the porous interface layer (3) using the support as an etch mask. This step is preferably executed by under-etching using a chemical etching solution that selectively attacks the electroless porous Si or oxidized porous Si but does not attack substantially the Si semiconductor layer. By doing so, no surface damage is introduced at the thin film solar cell surface that was attached before to the substrate. However, the formation of the Si thin film can also result in a coverage of the edge regions of the substrate. In that case there is no direct access for chemical solutions to the porous Si layer or oxidized porous Si layer. Therefore, the Si thin film is removed (fig.1 l)) at the edge regions, preferably by grinding, etching or cutting, before the substrate can be detached. Alternatively this access can be achieved by applying the same techniques already at the beginning of the process directly after the thin film growth. This allows to diffuse also the edge regions when this seems favorable or beneficial for the final cell performance.

A method of selectively removing the porous interface layer (3) will now be described which is advantageous for an oxidized porous layer. After CVD deposition of Si thin film layer, processing a solar cell into the thin film and attaching a final

support substrate, the thin film device with the attached support substrate is detached from the Si host substrate. This is preferably done by underetching the porous silicon oxide layer in a solution that contains a high concentration of hydrofluoric acid (HF). This can either be a buffered HF solution containing for instance  $\text{NH}_4\text{F}$  or only a mixture of HF and  $\text{H}_2\text{O}$ . HF removes selectively the oxidized porous Si layer and does not etch the Si host substrate and the thin film solar cell. Under-etching of a porous Si layer occurs at a considerably higher etch rate than the etching of a dense  $\text{SiO}_2$  film on bulk Si. The etch rate of oxidized porous Si is typically more than 1000 times faster than that of  $\text{SiO}_2$ . The higher the concentration of HF, the higher will be the etch rate. Therefore, it is a preferred embodiment to use a 50% HF concentration. This solution can be used for many under-etching cycles of a great many substrates without replenishment and is therefore does not contribute much to the processing cost. Furthermore, recycling of the solution is facilitated if a pure HF solution (50 %) is used.

A further method of underetching the porous layer which may advantageously be used when this layer has been doped to reduce porosity gradient will now be described. After attaching a support substrate to the processed thin film solar cell, the substrate is immersed in a selective etching solution to under-etch the porous Si layer from the edges of the substrate. The support substrate acts as an etching mask and the Si host substrate and Si thin film device will not be etched substantially. Typical etching solutions may be caustic alkaline etchants in low concentrations. These etchants comprise for instance potassium hydroxide (KOH), sodium hydroxide (NaOH), ammonium hydroxide  $\text{NH}_4\text{OH}$  or calcium hydroxide  $\text{CaOH}$ . Normal concentrations of below 1 mol/liter are advised for all of these caustic etchants. More specifically, low concentrations of around 0.1 mol/liter are preferred. These solutions allow to a selectivity in the etch rates for bulk Si and porous Si. This selectivity is preferably so pronounced that the etch rate of porous Si at the areas of high porosity is at least 10000 times faster than that for bulk Si. Preferably the etch rate should be more than 100000 times faster for porous Si than for bulk Si. It is possible to co-process in these solutions large batches of wafers and to use the solutions for a large number of substrates by replenishing the mentioned caustic alkaline etchants.

Furthermore, solutions containing mixtures of hydrogen peroxide with sulfuric acid or with ammonium hydroxide can be used for the selective under-etching. These

solutions only oxidize the topmost part of a Si surface. In the case of porous Si however they cause a very strong reaction due to the high surface area of porous Si and remove therefore the porous layer at the interface of high porosity. In this way a complete selectivity in etching can be achieved.

5           After separation, the interconnection strips for module assembling of the thin film solar cells can optionally be attached by soldering prior to the attachment of a support or by creating openings in the support to access the busbars of both electrode metallisation patterns.

10           After detachment of the completed solar cell structure the surface that was before in contact with the substrate is still basically unpassivated. Therefore an additional  $\text{SiN}_x$  or  $\text{TiO}_x$  deposition can be performed (fig.1 n)) on this surface. If plastic or other organic materials are used as a support the deposition temperature for these materials has to be adapted. Experiments show that temperatures down to 150 degrees C still allow for the deposition of uniform and homogeneous passivating layers  
15 (15) that might serve at the same time as anti-reflective coating (ARC) layer when this surface of the thin film solar cell is used as front surface. For simplicity the figures and the description are limited to only one half of the substrate. Obviously the process is suited to form symmetrically on both major surfaces of the carrier substrate exactly the same structures.

20           Which of the surfaces is to be used as the front surface depends strongly on the quality of the deposited thin film layer and the respective minority carrier life time after processing, on the final active device thickness, on the light trapping behavior and on the shading losses related to the metallisation patterns in case the metallised surface is chosen to be the front surface. In the latter case the support has to be transparent.  
25           This transparent support might be for instance an ethyl-vinyl-acetate (EVA) that is laminated to the surface. EVA is typically used anyhow for module encapsulation and might serve directly as encapsulant.

          In a second embodiment of the present invention (figure 2), as a second example, the formation of the thin film is such that initially a very thin layer of n-type  
30           Si is grown (21). The thin film growth is then completed by a bulk layer of p-type Si material (22) and further processing is executed as described in the first preferred embodiment. One of the reasons to form such a thin n-type Si layer on the surface that is only accessible at the end of the process is to obtain a better passivation of this

surface because weakly doped n-type Si layers can be much easier and better passivated. At the end of the process, this n-type Si layer either results in a completely isolated floating junction or can still be connected via a relatively high resistive path over the edge regions of the thin film if the access to the porous layer underneath is opened before the diffusion process or in other words if the thin film is removed at the edge regions previous to n-type diffusion.

The use of such a thin floating junction can result in considerably improved values of the open circuit voltage. This is of particular interest if this surface is the illuminated front surface and if the bulk thickness of the thin film is smaller than the minority carrier diffusion length. However also when the thin film solar cell is not used as back contact solar cell and the metallised surface is illuminated, the illumination level for really thin solar cells with good light trapping behavior will be still considerably higher than for conventional thick crystalline Si solar cells and therefore benefits from a floating junction passivation can be more pronounced.

In a third embodiment of the present invention (figure 3), as a third example, the formation of the thin film is such that a Si multi-layer is formed comprising at least two Si layers of opposite doping type which define a p-n junction being located in the bulk of the thin film but sufficiently close to the exposed surface of the thin film surface in order to allow that this p-n junction can be reached by local diffusions from the exposed surface. Such structures are of particular interest when minority carrier diffusion lengths smaller than the device thickness are encountered at the end of the thin film solar cell fabrication process. One can either start with the formation of an n-type or a p-type doped layer on the porous silicon layer and continue with an opposite doped layer on top. Both options seem to be feasible.

As a first option, figure 3 a), according to this third embodiment of the invention the thin film deposition starts with the deposition of a n-type layer (31) on the substrate (1), that has a porous layer (3) on it's textured surfaces (2) as previously described. By switching to another doping ambient subsequently a p-type layer (32) is deposited. Finally a selective diffusion is used to form the n-type layer (7) that is weaker doped than the selectively heavily and deeply doped regions (33) that are formed during a selective diffusion step. The diffusion at these areas penetrates that deep in the substrate that the p-type layer (32) gets locally over-doped by n-type doping atoms. By doing so access is provided to the still deeper n-type layer (31). The



deep n-type layer, the deeply n-type doped region (33) and the weakly doped n-type surface layer (7) are all electrically connected and contacted by means of a metal connection (12) (preferably by screen printing an Ag paste). The other processing steps can be executed according to the first embodiment of this invention. The resulting structure differs from the one described in figure 2 because now all three layers of the n-p-n stack are actively contributing to the collection of minority carriers. In that way the collection volume of the thin film solar cell can be increased particularly in case the minority carrier diffusion length is smaller than the device thickness.

Particularly the n-type layer (7) and the n-type doped regions (33) can be formed by selectively printing a diffusion paste while other areas can be masked from diffusion by a masking paste for instance. During the diffusion step, those areas that received diffusion paste will get heavily diffused resulting in  $n^{++}$  region (33) that have to penetrate through the p-type Si layer. Penetration depths in the order of  $1\mu\text{m}$  can be easily achieved when using a phosphorous paste and the grown junction can consequently be located  $1\mu\text{m}$  below the surface giving still local access to the buried grown n-type Si bulk layer (31). All areas that were neither covered by the diffusion paste nor by the masking paste will get weakly and shallow doped n layers (7). This is again due to the indirect diffusion via the gas phase, mentioned earlier. This allows consequently to have all major surfaces n-type again which is advantageous to obtain an effective passivation. This results basically in a structure with a p-type layer sandwiched between two n-type layers, having all three layers connected to electrode terminals on the processing surface.

As a second option, figure 3 b), according to this third embodiment of the invention the thin film deposition starts with the deposition of a thin n-type floating emitter layer (35) on the substrate (1), that has a porous layer (3) on its textured surfaces (2) as previously described. This is followed by deposition of a p-type layer (36), an n-type layer (37) and another p-type layer (38). During a subsequent diffusion step, two diffusion pastes of opposite type are used. The p-type regions (39) get very deeply diffused, while the n-type regions (33) get just deeply enough n-type diffused to access the n-type layer (37). The weakly doped regions (7) are created in the same manner as in the previous embodiments. The p-type regions (39) used to access the buried p-type layer (36) can be formed either during diffusion using a paste with a p-type doping impurity as Al, Ga or B or only at the end of the solar cell processing

sequence using an Al paste for metallisation. Al alloys very fast with Si already at temperatures above the eutectic temperature of about 580 degree C and can be used to penetrate locally deeply (high diffusion rate) inside the Si layers. This allows to locate the device junction at virtually any desired location of the thin film as for instance at half of its thickness having still the possibility to connect the buried p-type layer to the metal grid that will be formed on the surface that is accessible for processing before lifting off the thin film solar cell. The  $p^{++}$  regions of Al alloys can penetrate easily 20  $\mu\text{m}$  or more if required. These regions should be well separated from the  $n^{++}$  regions (33). The grown n-type Si layer (37) should be of rather high resistivity to avoid shunt paths to the  $p^{++}$  regions (39). The possibility to locate the grown junction plane at virtually any desired location parallel to the surfaces can give the same advantages as described in the discussion of fig.3 a). Furthermore, positioning the junction in the middle of the device might be an advantage due to the increase of the accessible collection volume of the device which can result in better conversion efficiencies of the thin film solar cell.

In case no optional n-type layer (35) is formed on the porous Si layer, then the p-type surface that is in contact with the substrate during processing might not be easy to passivate when using the same processing sequences to finish the solar cell as described in the previous embodiments. In case an additional thin n-type layer (35) is formed then this layer can be either completely floating or connected via a diffusion along the edge of the thin film as already described in embodiment 2. All other processing steps as diffusion, passivation and metallisation can be executed basically in the same way as described in the previous embodiments.

In a fourth embodiment of the present invention (figure 4), as a fourth example, the formation of a multi Si layer thin film is such that a thin film Si solar cell is formed comprising a plurality of parallel collecting junctions in the bulk of the device. Particularly, when the used deposition techniques for thin film formation result only in Si layers of modest quality and lower minority carrier diffusion lengths than the device thickness, it is advantageous to have as many as possible parallel collecting junctions in the bulk of the device in order to increase the responding collection volume clearly. Figure 4 depicts such a multi Si layer thin film device with a plurality of n-type layers (41) and p-type layers (42) that are all formed by Si deposition in alternating doping source ambients. Such an alternated deposition could occur at different locations in a

quasi-continuous deposition system without having to ramp the temperature up and down between the consequent individual deposition steps. To connect all individual layers to the surface that is metallised by the contacts (12) and (13) as for previously described cells, a deep local diffusion of both doping impurity types is required to form the highly doped connection regions (43) and (44). The fabrication of such connection regions without shunting the solar cells is quite difficult. This can be done by applying selectively the diffusion sources of the respective type as for instance by screen printing doping pastes and using masking paste to avoid lateral cross diffusion. Care has to be taken that during the diffusion no excessive cross doping will occur between the grown Si layers of different doping type since the thickness of each of this layers is substantially smaller than the device thickness through which the local diffusions extend. Therefore the use of different doping impurity atoms during the thin film growth process and for the local diffusions seems to be unavoidable. Doping impurities like Al and P, that diffuse at reasonably low temperatures comparably fast through Si, have to be used in diffusion pastes for the selective formation of the connection regions. Doping impurities like B and Sb that diffuse at typical diffusion temperatures only slowly are preferably used for doping the various Si layers during the Si thin film growth. The various n- and p-type Si layers should be preferably weakly doped to avoid lateral shunt paths in the Si bulk between the different strongly doped connection regions that will be metallised.

It should be stressed once more that the present invention is by far not limited to Si solar cell devices as discussed in the previous embodiments. Other semiconductor materials can be used as well. Combinations of different semiconductor layers seem attractive as well. For instance a stack of Si and SiGe layers could offer an interesting tandem solar cell device. Si layers could serve for better surface passivation, while sandwiched thin SiGe layers very closely spaced from the front surface could offer a better choice in converting highly energetic photons. The layers can be grown in the same way as the previously described junctions can be grown, i.e. by switching the gas atmospheres during deposition.

Furthermore, other semiconductor devices such as diodes or power devices can be fabricated according to the method of the present invention to drastically reduce the overall cost by using a comparably cheap Si thin film on a cheap substrate without increasing processing cost considerably.

## WHAT IS CLAIMED IS:

1. A method for fabricating thin film semiconductor devices on a reusable substrate of a semiconductor material comprising the steps of:

5        providing a substrate of a semiconductor material having at least one surface;  
      forming at least one porous layer on said surface of said substrate;  
      depositing at least one semiconductor layer on said porous layer;  
      forming active devices in said semiconductor layer;  
      forming electrical contacts to said active devices;  
10       attaching a support to the surface overlying said metal connections; and  
      non-mechanically detaching said substrate from said semiconductor layer by  
      removing said porous layer with a wet chemical etch using said support as an  
      etch mask.

15    2. A method as recited in claim 1, wherein said porous layer on said surface of said  
      substrate is formed by an electroless etching technique in an aqueous chemical  
      solution.

20    3. A method as recited in claim 1 or 2, wherein said surface of said substrate is  
      textured or structured prior to forming said porous semiconductor layer.

4. A method as recited in any of claims 1 to 3, wherein said support is a flexible sheet  
      material.

25    5. A method according to any previous claim, wherein said support is composed of a  
      plastic or a polymer.

6. A method according to any previous claim, wherein said porous layer is a single  
      porous semiconductor layer.

30    7. A method as recited in claim 6, wherein said single porous semiconductor layer is  
      formed such that there is a gradient in porosity.

8. A method as recited in claim 6 or 7, wherein said porous semiconductor layer is a porous silicon layer, said method further comprising the step of thermally oxidizing said porous silicon layer to thereby convert said porous silicon layer to a porous silicon oxide layer.

9. A method as recited in claim 8, wherein said substrate is detached from said semiconductor layer by removing said porous silicon oxide layer using a wet chemical etch, said wet chemical etch being selective to said substrate and said semiconductor layer.

10. A method according to any previous claim, wherein said active devices comprise at least one n-type doped region and at least one p-type doped region being formed in said semiconductor layer and having an exposed surface, and wherein said n-type region and said p-type region of said active devices are contacted at said exposed surface by said metal contacts.

11. A method as recited in claim 10, wherein said metal contacts are formed by screen printing a first metal paste to contact said p-type doped regions and a second metal paste to contact said n-type doped regions.

12. A method according to any previous claim, wherein said semiconductor material of said substrate is selected from the group consisting of Si, SiGe, Ge, GaAs.

13. A method as recited in claim 12, wherein said substrate is doped with either an n-type impurity or a p-type impurity, said substrate having a highly doped surface region whereon said porous layer will be formed.

14. A method according to any previous claim, wherein each of said semiconductor layers is either an n-type or a p-type doped layer being composed of a semiconductor material selected from the group consisting of Si, Ge, SiGe, GaAs.

15. A method as recited in claim 14, wherein said thin film semiconductor devices are thin film solar cells having a plurality of actively collecting semiconductor layers of

different doping types.

16. A method according to any previous claim, wherein after detaching said substrate an additional layer is formed on exposed parts of said semiconductor layer, said  
5 additional layer being used at least as a passivation layer or an anti-reflective coating layer or a back surface reflector layer.

17. A method for fabricating thin film semiconductor devices on a reusable substrate of a semiconductor material comprising the steps of

10 providing a substrate of a semiconductor material having a first major surface, a second major surface, opposite to said first major surface, and edge surfaces;

forming at least one porous semiconductor layer on each of said major surfaces and said edge surfaces of said substrate by an electroless etching technique in an aqueous chemical solution;

15 depositing at least one semiconductor layer on said porous semiconductor layer;

forming active devices at least in the semiconductor layers formed on said first major surface of the substrate;

20 forming metal contacts at said first surface of said substrate contacting said active devices;

attaching a support to the surface overlying said metal connections;

removing at least the semiconductor layers formed at the edge surfaces of the substrate to thereby expose the edges of the porous semiconductor layers; and

25 non-mechanically detaching said substrate from said semiconductor layer by removing said porous layer with a wet chemical etch using said support as an etch mask.

18. A method as recited in claim 17, wherein thin film semiconductor devices are fabricated both in the semiconductor layers formed on said first major surface of the  
30 substrate and on said second major surface of the substrate.

Figure 1

Fig. 1a):

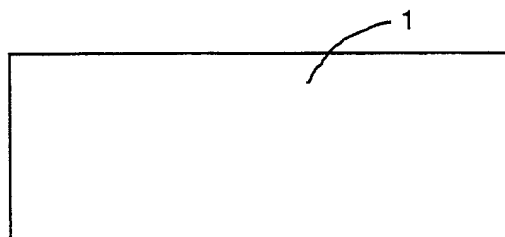


Fig. 1b):

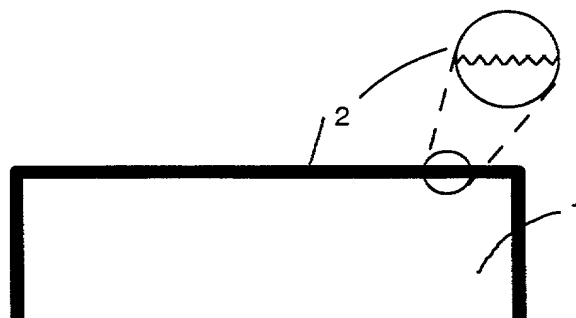


Fig. 1c):

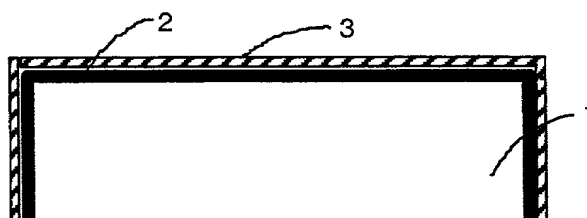


Fig. 1d):

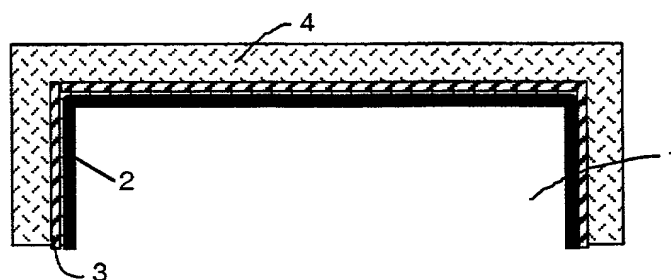
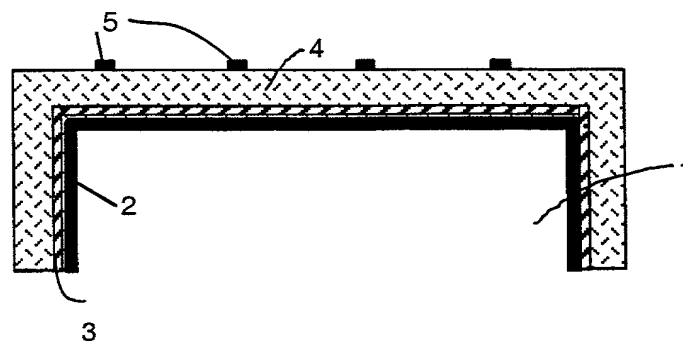


Fig. 1e):



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Fig. 1f):

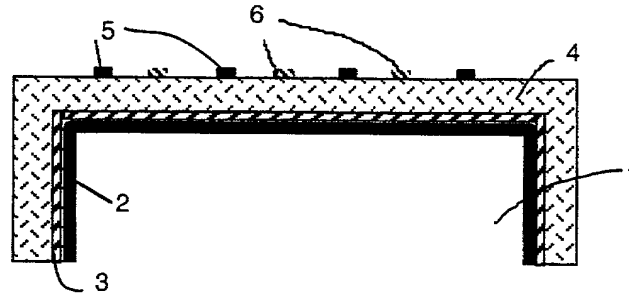


Fig. 1g):

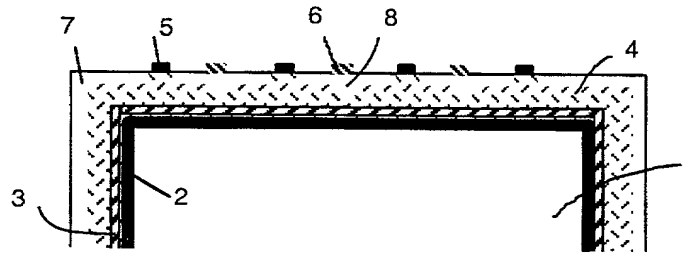


Fig. 1h):

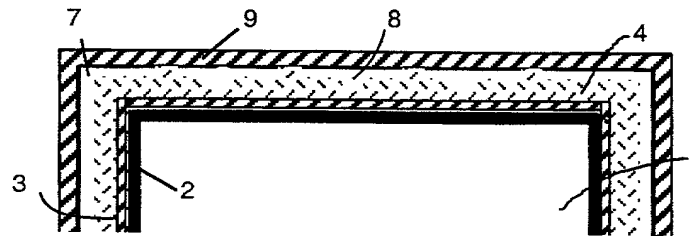


Fig. 1i):

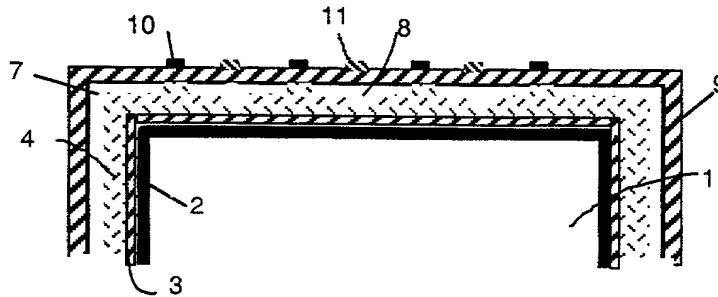
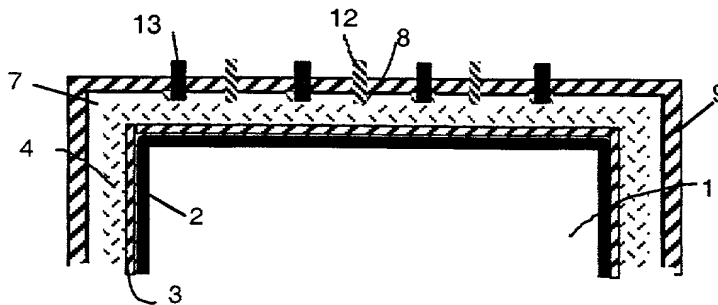
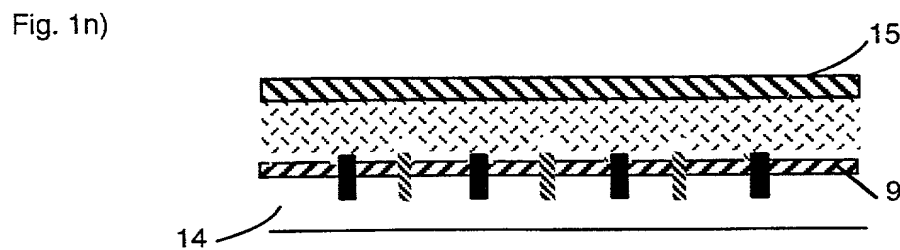
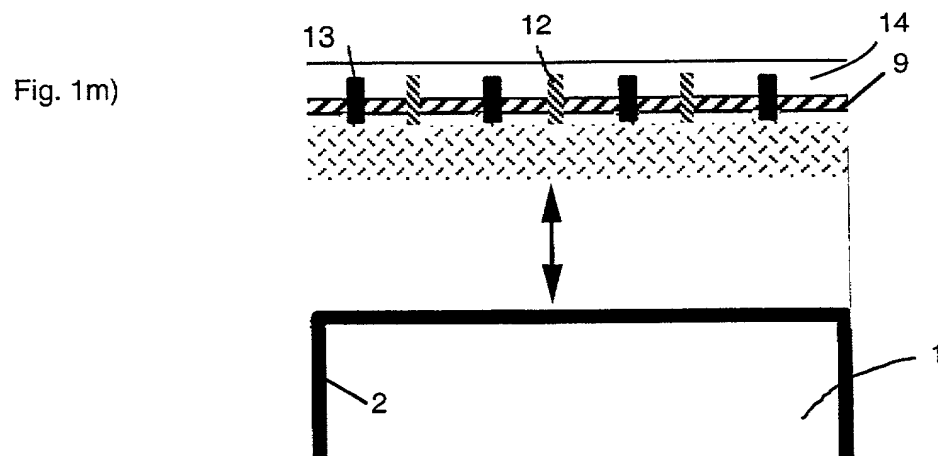
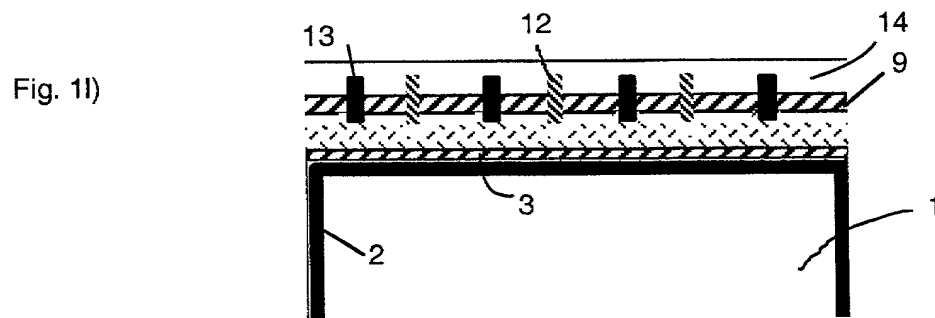
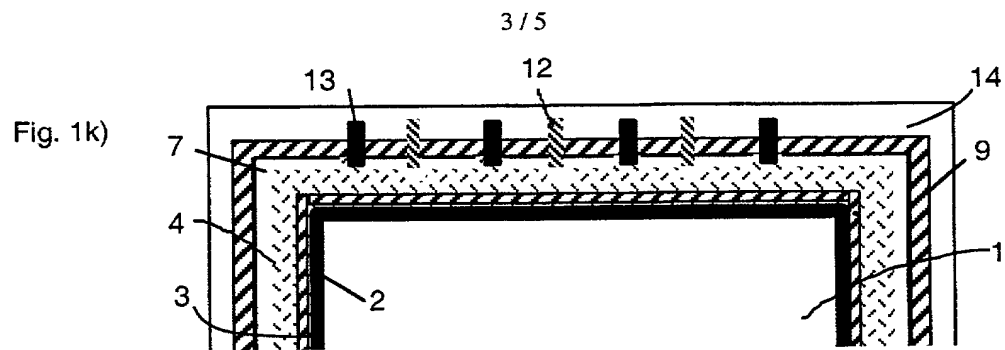


Fig. 1j):







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Figure 2

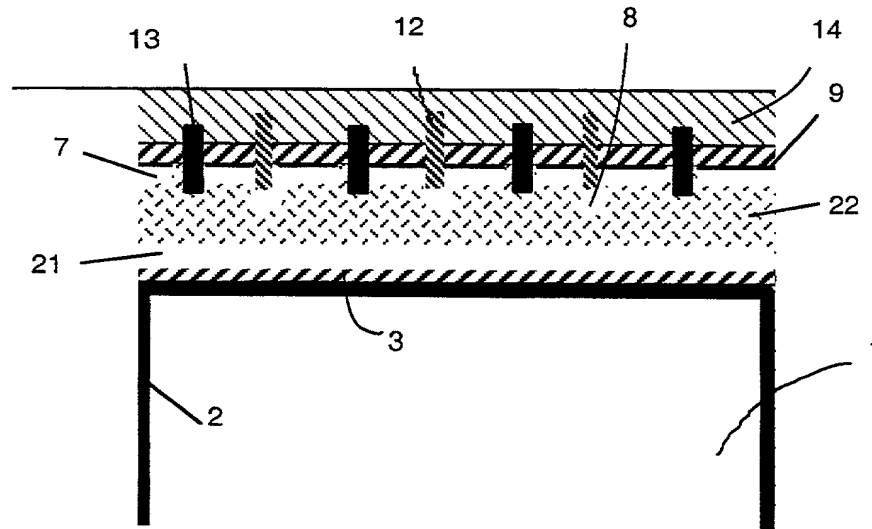


Figure 3

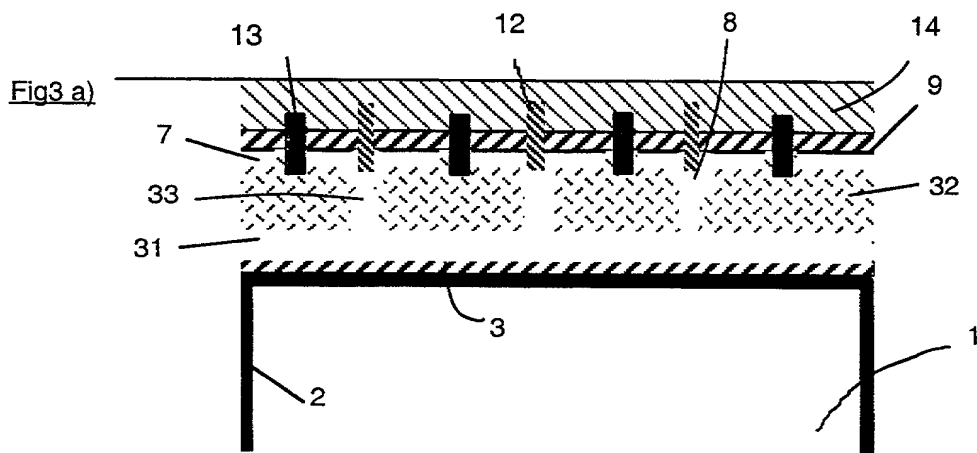


Fig 3b)

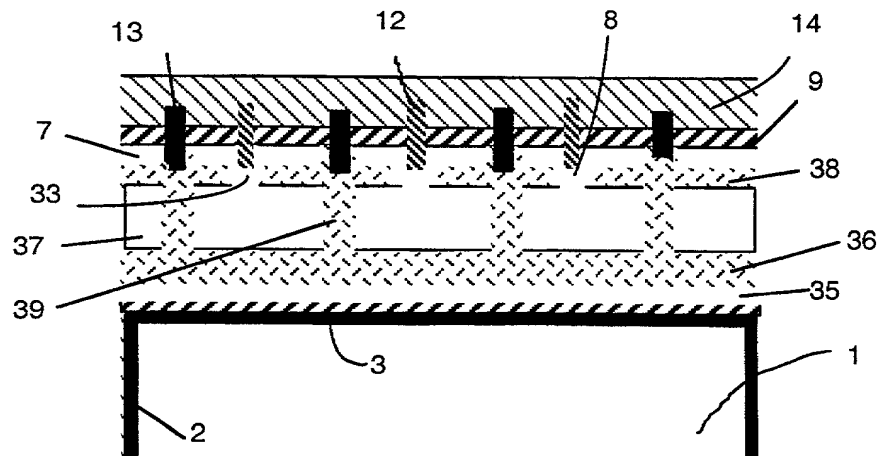
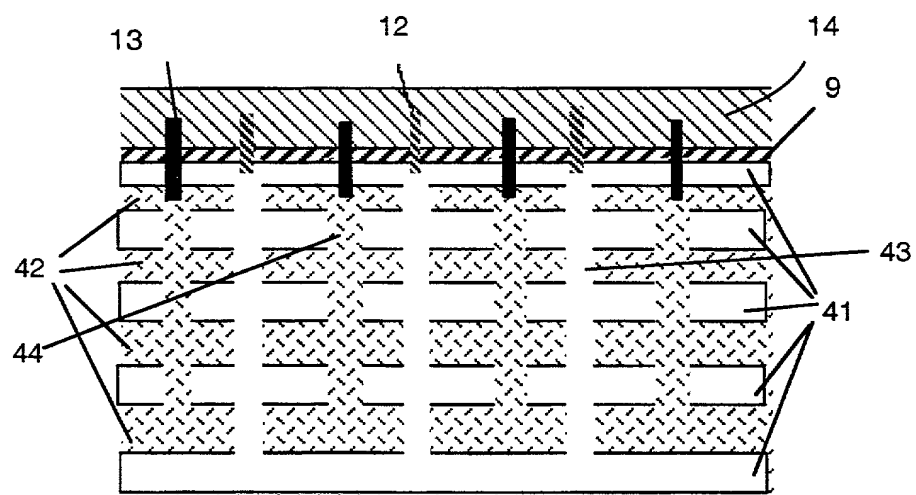


Figure 4





Docket No. 0522-1752

**DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION**

a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Method For Fabricating Thin Film Semiconductor Devices, the specification of which:

is attached hereto.

☒ was filed on 26 Jan 2002 as Application Serial No. PCT/EP00/00586  
and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

**PRIOR FOREIGN APPLICATION(S)**

Country	Number	Date Filed	Priority Claimed	
			Yes	No
Europe	99200235.2	27 January 1999	X	



[illegible]

And I hereby appoint Robert F. I. Conte, Registration No. 20,354, Thomas E. Smith, Registration No. 18,243, Dennis M. McWilliams, Registration No. 25,195, James R. Sweeney, Registration No. 18,721, William M. Lee, Jr., Registration No. 26,935, Glenn W. Ohlson, Registration No. 28,455, David C. Brezina, Registration No. 34,128, Jeffrey R. Gray, Registration No. 33,391, Timothy J. Engling, Registration No. 39,970, Gerald S. Geren, Registration No. 24,528, Peter J. Shakula, Registration No. 40,808, Wm. Marshall Lee, Registration No. 16,853, and Gregory B. Beggs, Registration No. 19,286 to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith. It is requested that all communications be directed to:

\_\_\_\_\_

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Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Jörg Horzel

Signature Jörg H. Horzel Date 7. 8. 2001

Country of Residence: Germany

Country of Citizenship: Germany

Post Office and Residence Address: Hertogstraat 47, B-3001 Leuven, Belgium

Full name of joint inventor: Eva Vazsonyi

Signature Eva Vazsonyi Date 7. 8. 2001

Country of Residence: Hungary

Country of Citizenship: Hungary

Post Office and Residence Address: Torocko utca 20, H-1026 Budapest, Hungary